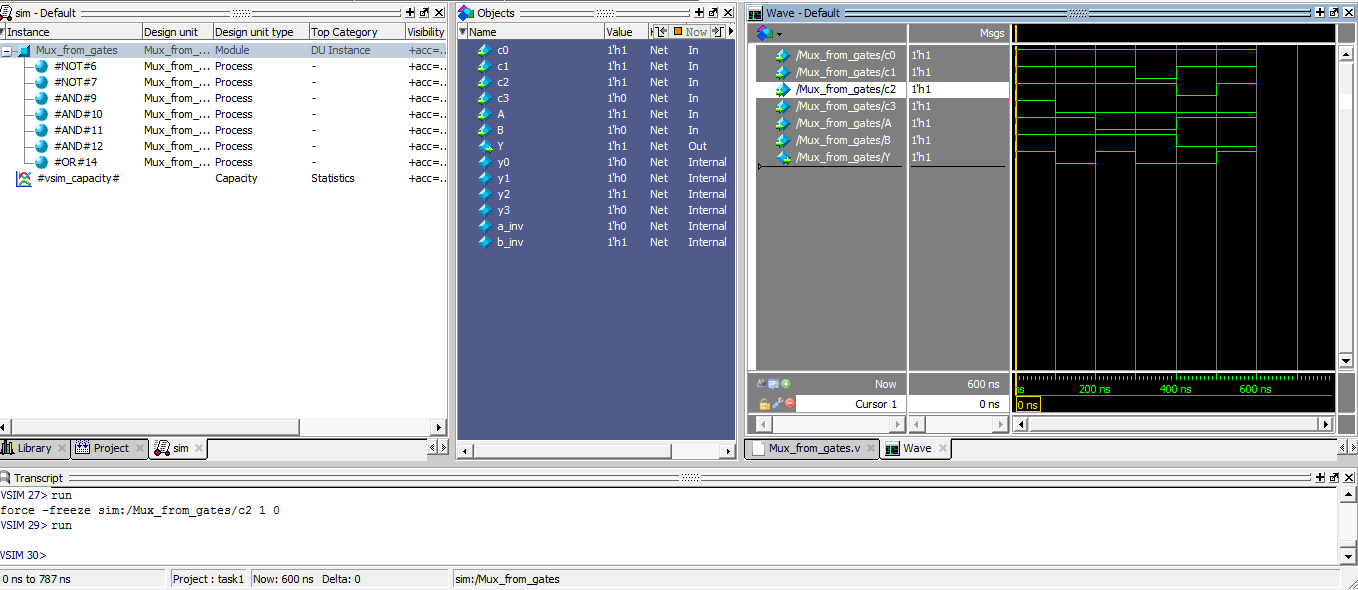
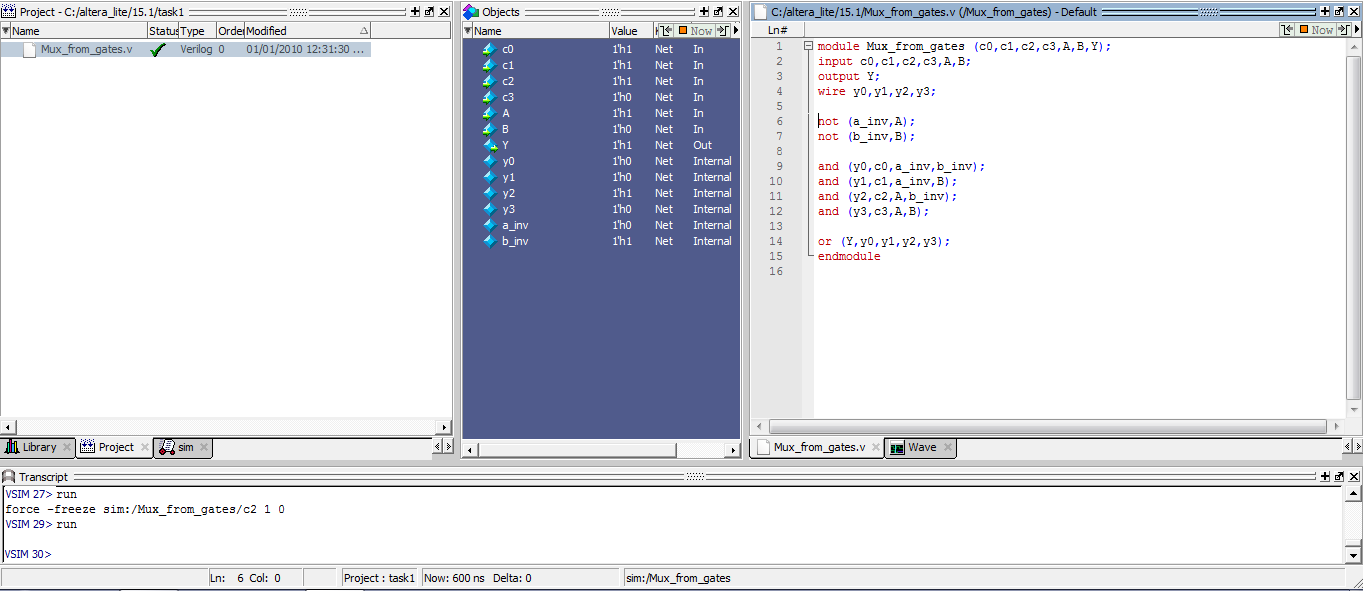
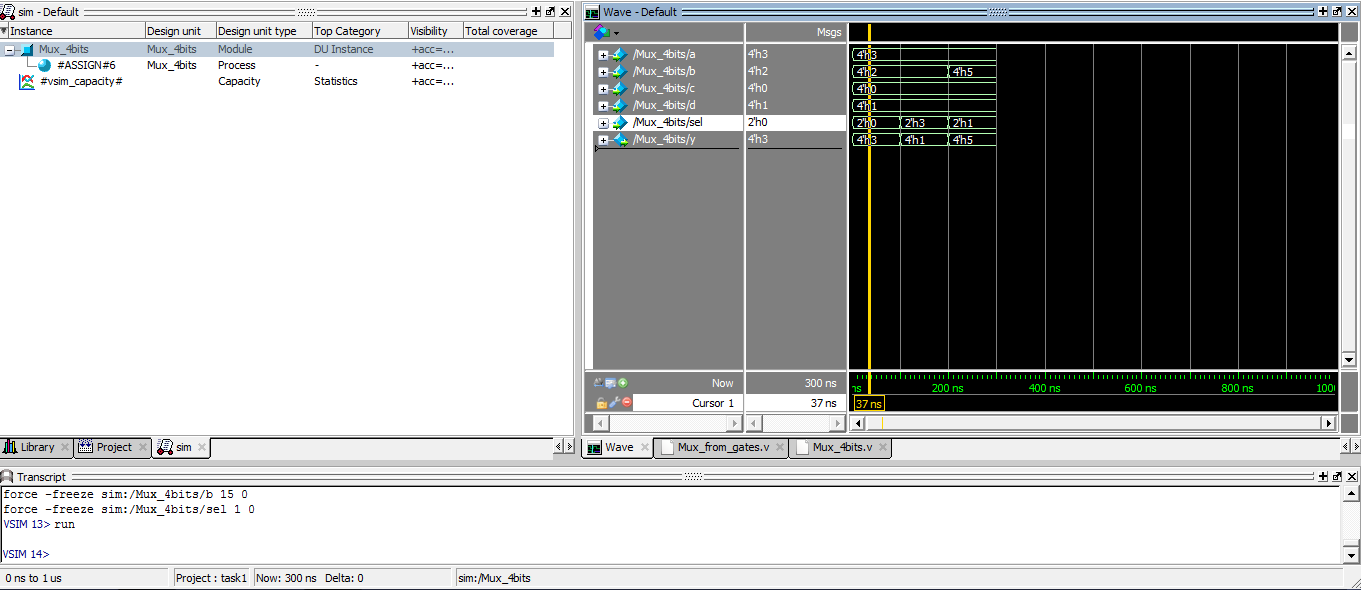
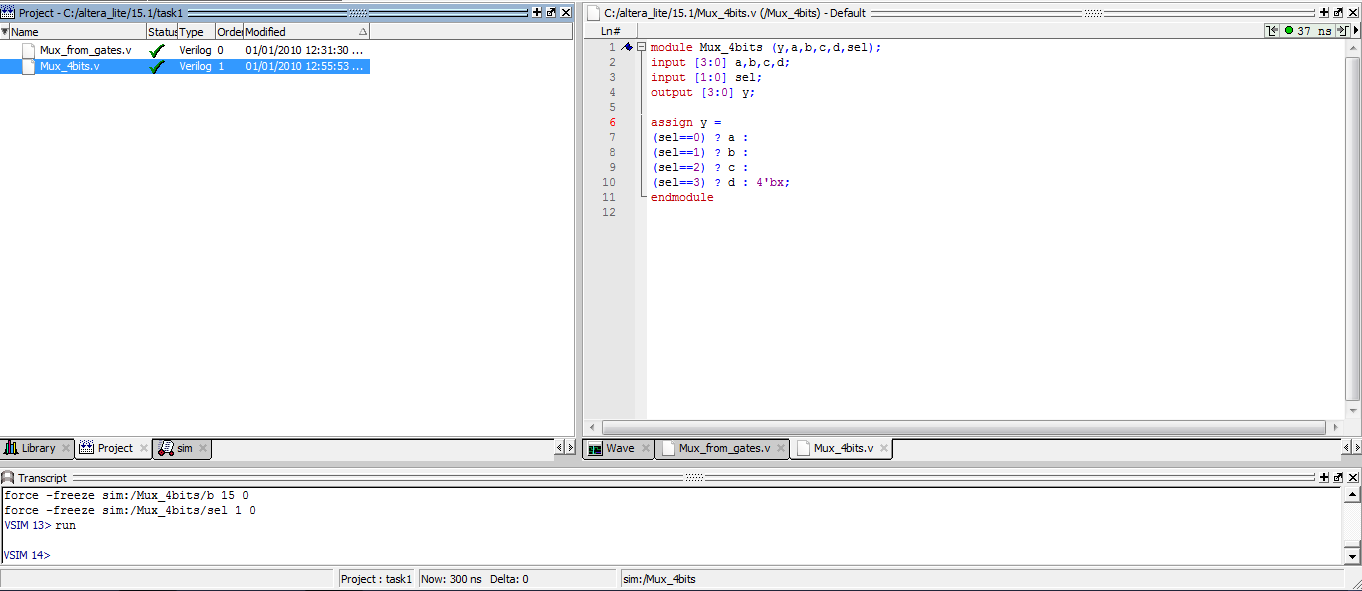
1 – multiplixer 1 of 4 lines with 2 selectors



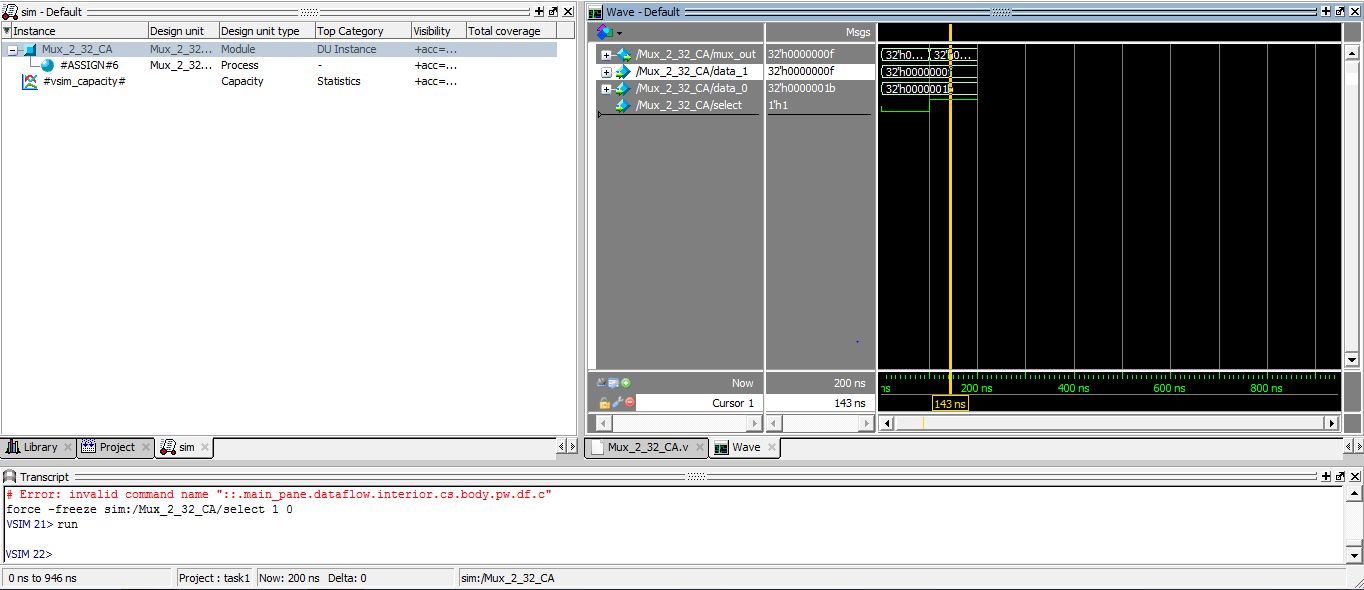


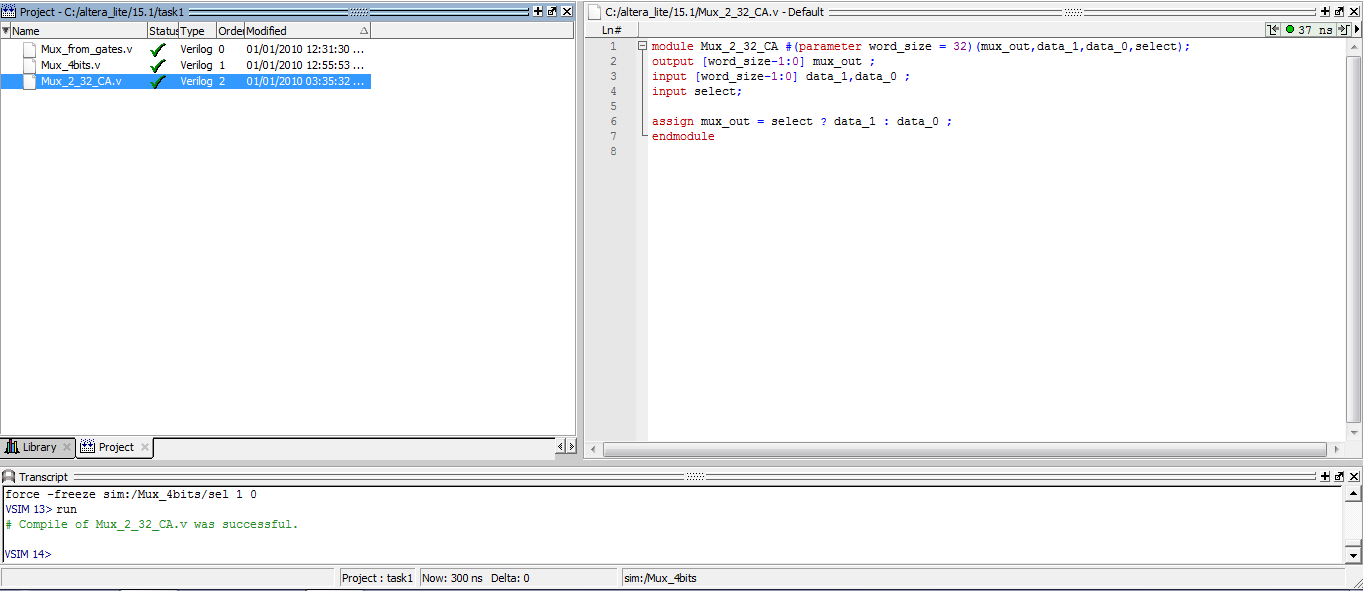
2- multiplixer 1 of 4 data line (each one is 4 bits data line) with selector (2 bits)



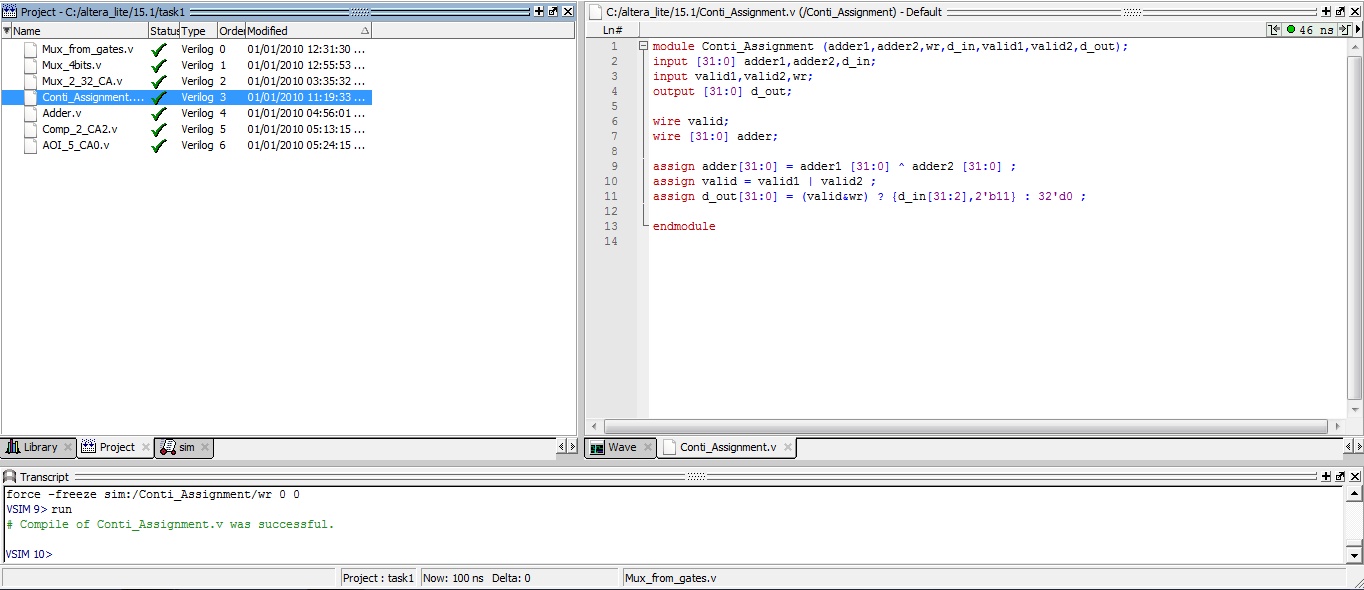


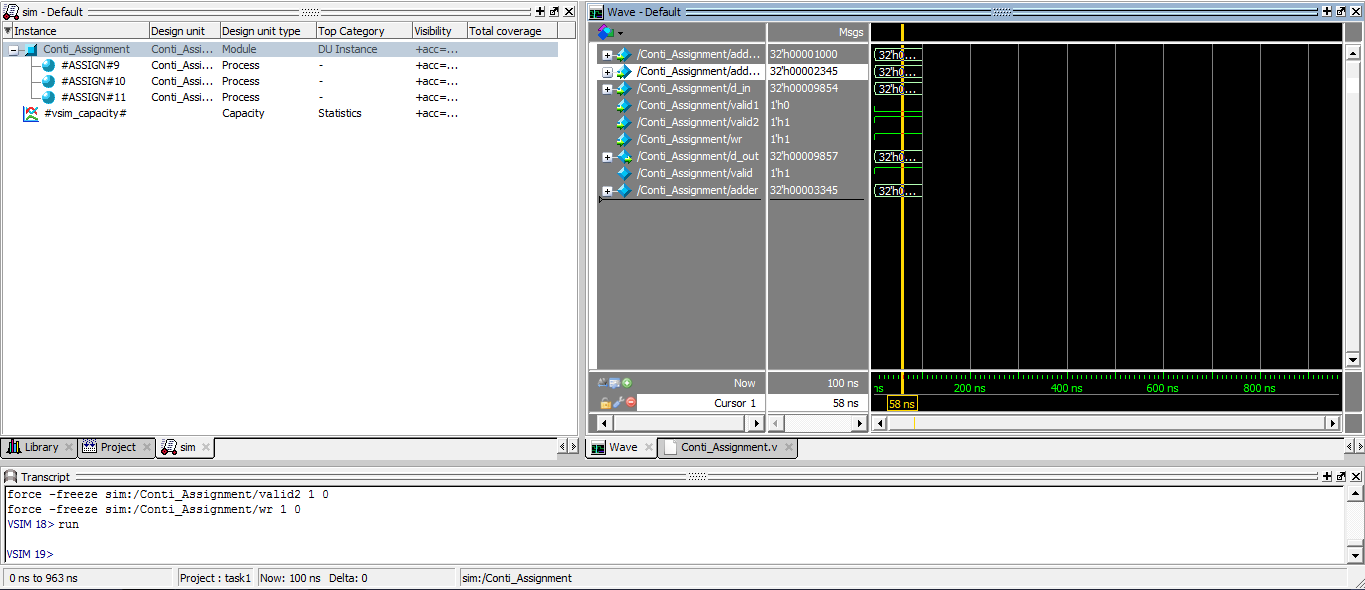
3- multiplixer 1 of 2 data line (each is 32 bits) with selector (1 bit)



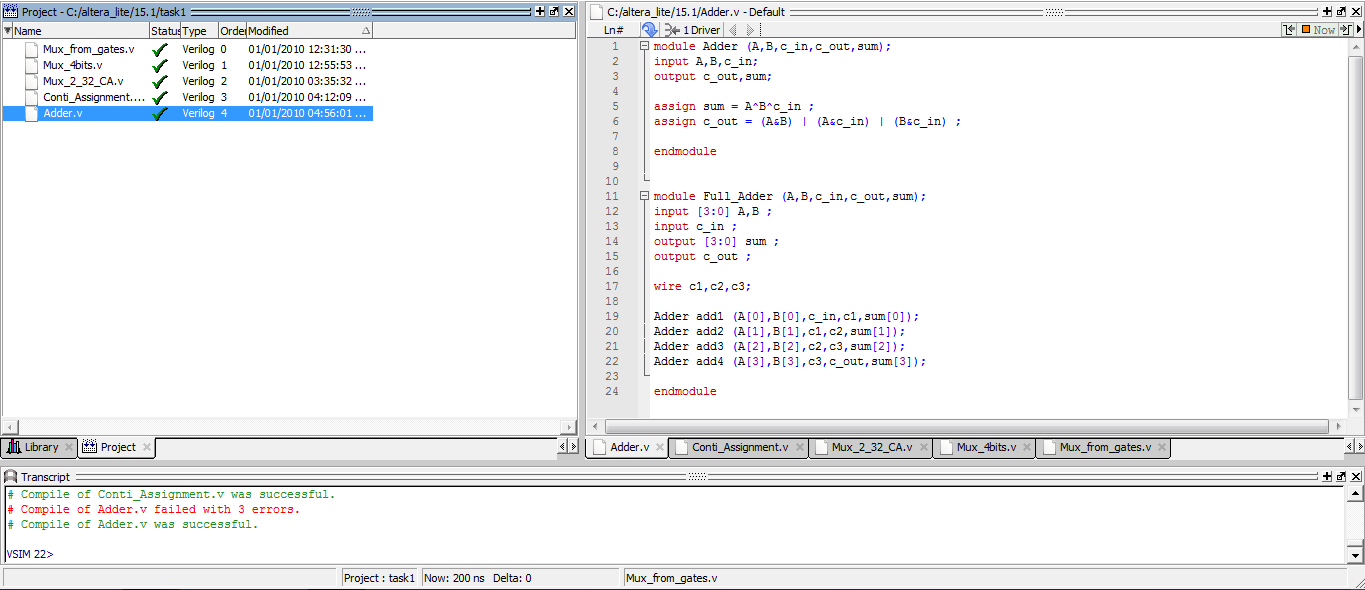


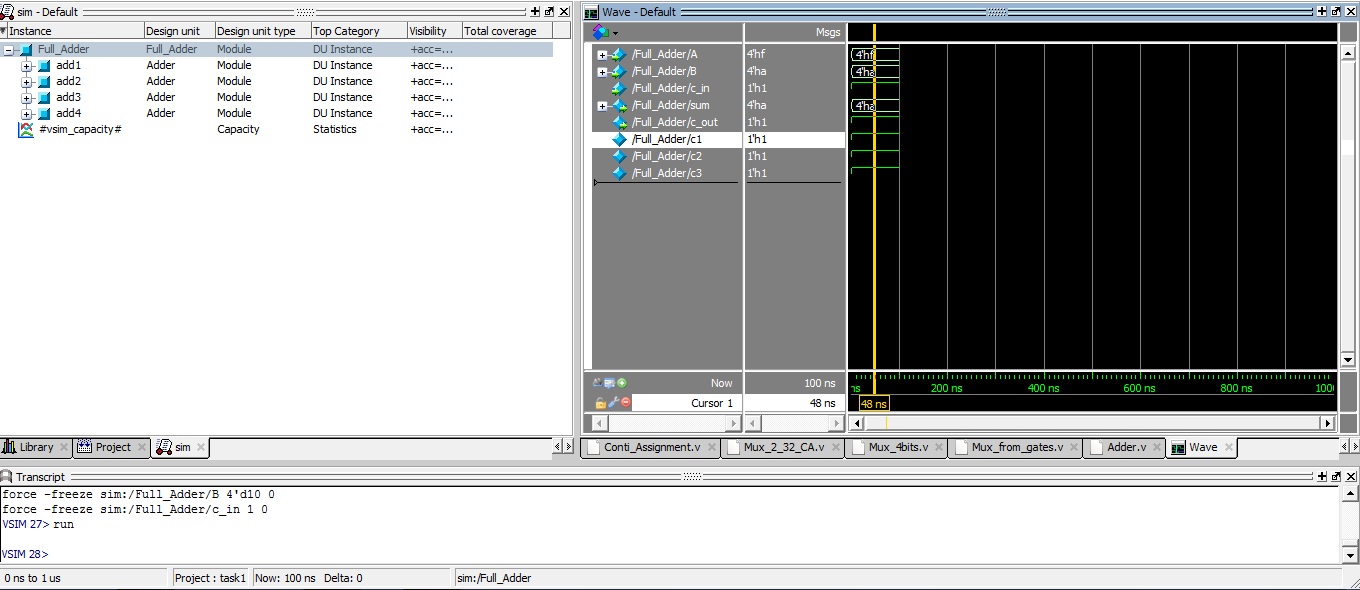
4- combinational logic circuit (anding and oring and xoring)



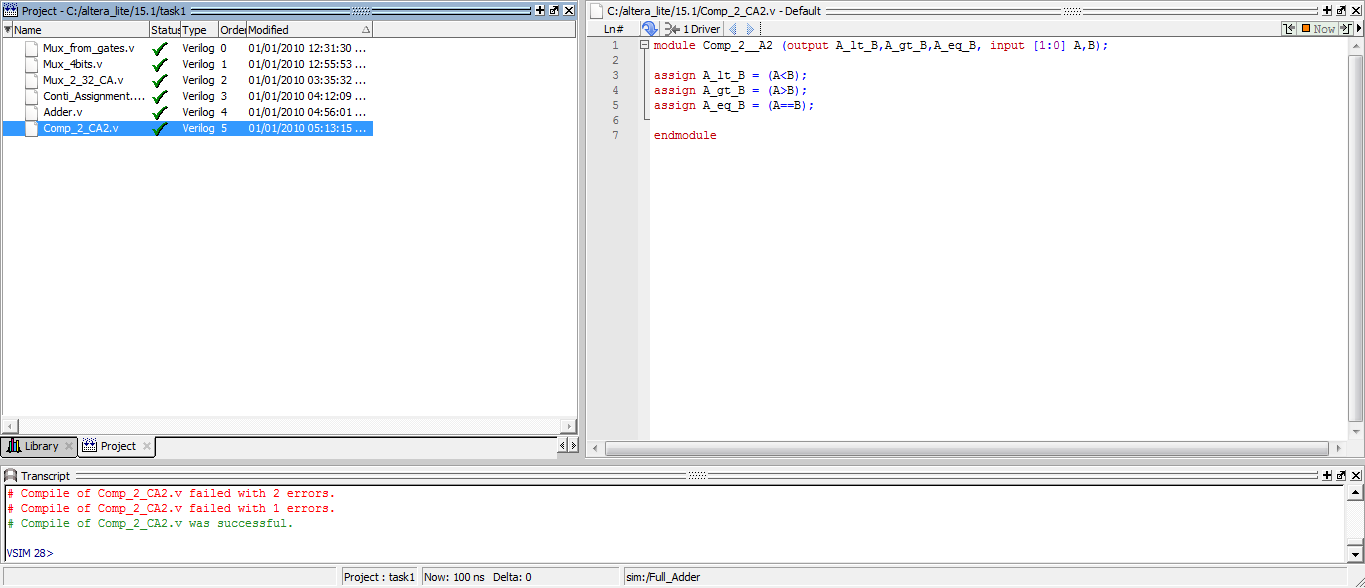


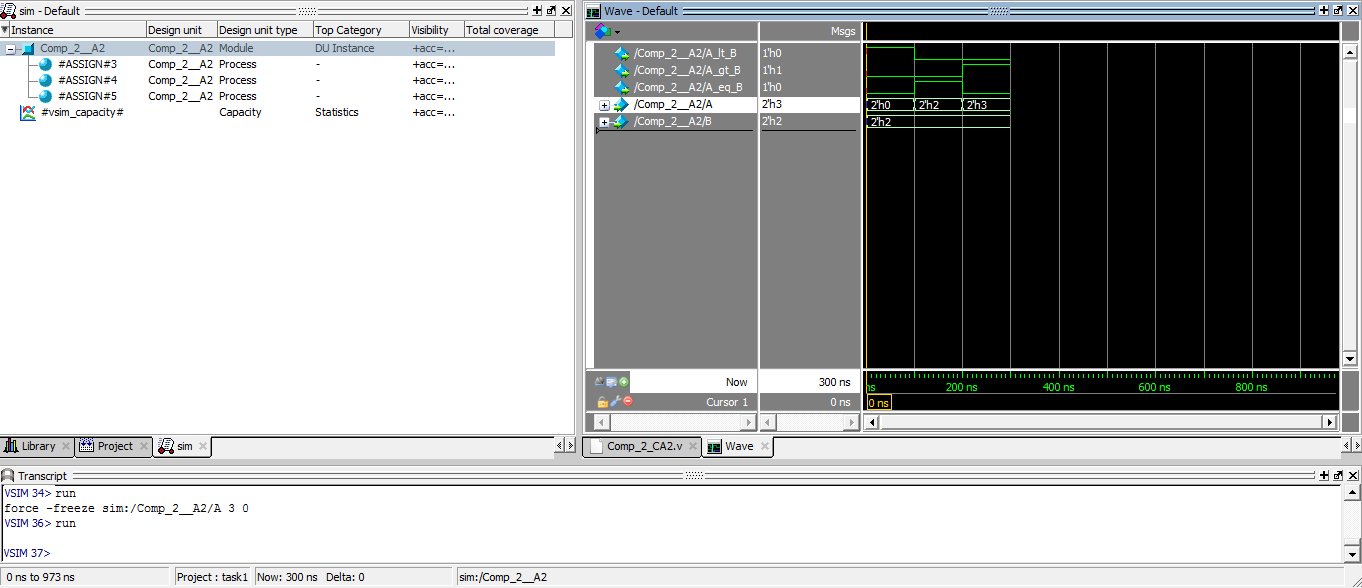
5-full adder from 2 half adders



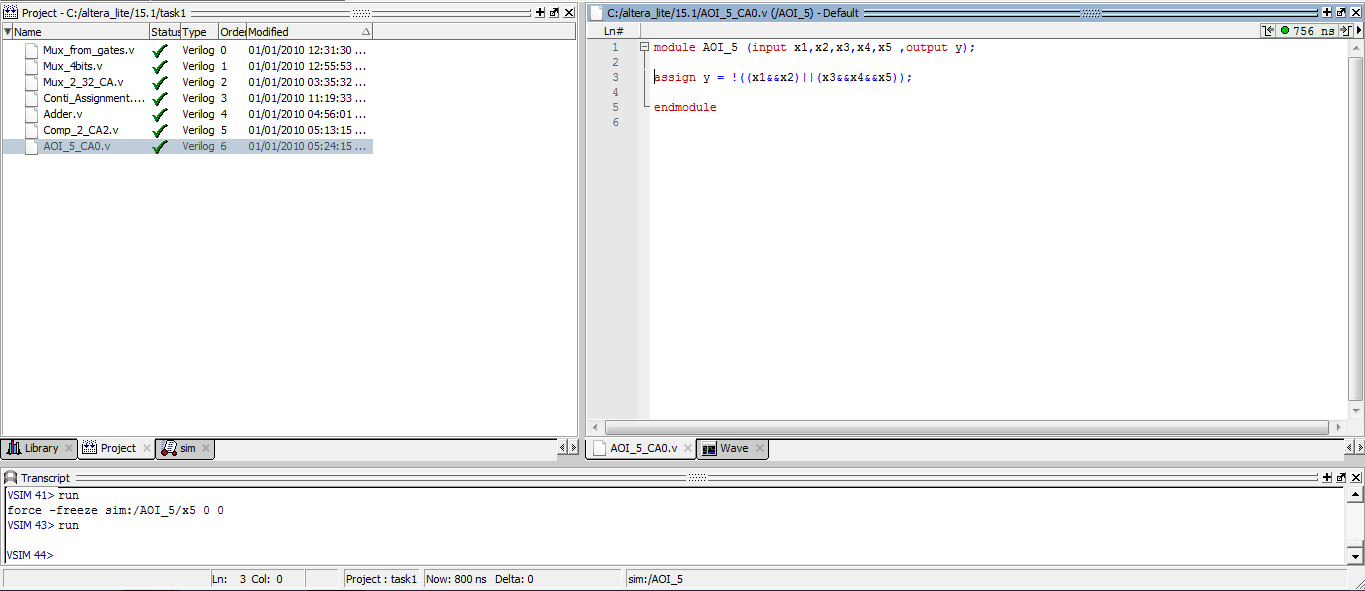


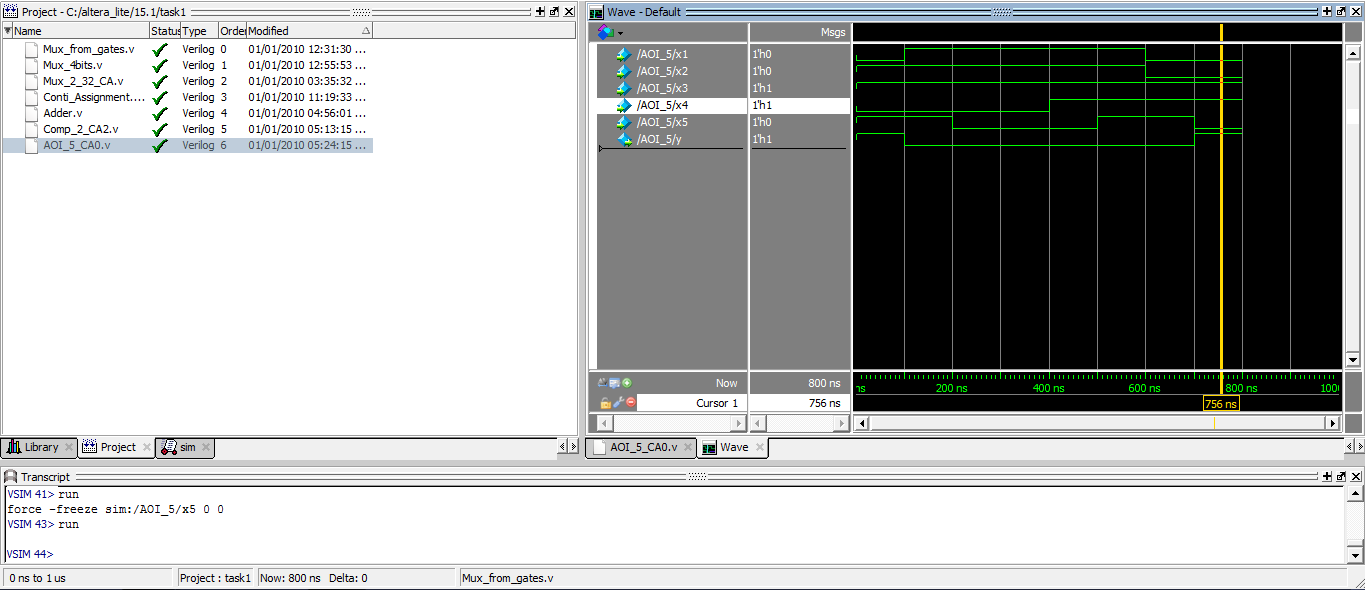
6-comparator between 2 input (each is 2 bits )





7- combinational logic circuit (anding and oring and not) (5 inputs each is 1 bit)





8- decoder 3 to 8

